

Note: For viewing my total publications including IEEE and non-IEEE publications, books, patents etc (Total: 340), please click here:

<https://www.anirban-sengupta.com/research.php>

This document only lists my IEEE publications

Total IEEE Publications (Journals + Conferences): 180

IEEE Journals: 84 (including *IEEE Transactions: 26*)

IEEE Conference Proceedings: 106

Author of papers in top venues of IEEE, Nature, ACM and IET - TVLSI, TCAD, TDSC, TCE, TAES, D&T, ESL, CASM, ITPro, CEM, Nature Scientific Reports, LOCS, Access, VCAL, Potentials, CDT, EL, ISQED, SOCC, AsianHOST, GLSVLSI, ISVLSI, ISCAS, DFTS, ASP-DAC, ICCE, VLSID, ICM, VLSI-DAT

IEEE JOURNALS

1. **Anirban Sengupta**, Nabendu Bhui "Securing Hardware IP core for CE systems using Fingerprint Biometric Integrated with Microscopic Fingerprint Features and Design Encoded Hash", **IEEE Transactions on Consumer Electronics (TCE)**, Accepted, 2025
2. Mahendra Rathor, Aditya Anshul, **Anirban Sengupta**, "Securing Reusable IP Cores using Voice Biometric based Watermark", **IEEE Transactions on Dependable and Secure Computing (TDSC)**, Volume: 21, Issue: 4, Aug 2024, pp. 2735 - 2749
3. **Anirban Sengupta**, Rahul Chaurasia, Aditya Anshul "Robust Security of Hardware Accelerators using Protein Molecular Biometric Signature and Facial Biometric Encryption Key", **IEEE Transactions on Very Large Scale Integration Systems (TVLSI)**, vol. 31, no. 6, pp. 826-839, June 2023
4. Rahul Chaurasia, **Anirban Sengupta** "Retinal Biometric for Securing JPEG-Codec Hardware IP core for CE systems", **IEEE Transactions on Consumer Electronics (TCE)**, Volume: 69, Issue: 3, pp. 441-457, Aug 2023
5. Mahendra Rathor, **Anirban Sengupta**, Rahul Chaurasia, Aditya Anshul "Exploring Handwritten Signature Image Features for Hardware Security", **IEEE Transactions on Dependable and Secure Computing (TDSC)**, Volume: 20, Issue: 5, pp. 3687 - 3698, Oct. 2023
6. **Anirban Sengupta**, Rahul Chaurasia "Secured Convolutional Layer IP Core in Convolutional Neural Network using Facial Biometric", **IEEE Transactions on Consumer Electronics (TCE)**, Volume: 68, Issue: 3, Aug 2022, pp. 291-306
7. **Anirban Sengupta**, Rahul Chaurasia, Tarun Reddy "Contact-less Palmprint Biometric for Securing DSP Coprocessors used in CE systems", **IEEE Transactions on Consumer Electronics (TCE)**, Volume: 67, Issue: 3, August 2021, pp. 202-213

8. **Anirban Sengupta**, Mahendra Rathor "Facial Biometric for Securing Hardware Accelerators", **IEEE Transactions on Very Large Scale Integration Systems (TVLSI)** , Volume: 29, Issue: 1, Jan. 2021, pp. 112 - 123
9. Wei Hu, Chip-Hong Chang, **Anirban Sengupta**, Swarup Bhunia, Ryan Kastner, Hai Li "An Overview of Hardware Oriented Security and Trust: Threats, Countermeasures and Design Tools", **IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems (TCAD)**, Invited Paper, Volume: 40, Issue: 6, June 2021, pp. 1010-1038
10. **Anirban Sengupta**, Mahendra Rathor "Obfuscated Hardware Accelerators for Image Processing Filters - Application Specific and Functionally Reconfigurable Processors", **IEEE Transactions on Consumer Electronics (TCE)** , Volume: 66, Issue: 4, Nov 2020, pp. 386-395
11. W Hu, CH Chang, **Anirban Sengupta**, S Bhunia, R Castner, H Li "Hardware Oriented Security and Trust", **IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems (TCAD)**, Accepted, 2021
12. **Anirban Sengupta**, Mahendra Rathor "Securing Hardware Accelerators for CE Systems using Biometric Fingerprinting", **IEEE Transactions on Very Large Scale Integration Systems (TVLSI)** , Volume: 28, Issue: 9, Sep 2020, pp. 1979-1992
13. **Anirban Sengupta**, Mahendra Rathor "Enhanced Security of DSP circuits using Multi-key based Structural Obfuscation and Physical-level Watermarking for Consumer Electronics systems", **IEEE Transactions on Consumer Electronics (TCE)** , Volume: 66, Issue:2, May 2020, pp. 163-172
14. Mahendra Rathor, **Anirban Sengupta** "IP Core Steganography using Switch based Key-driven Hash-chaining and Encoding for Securing DSP kernels used in CE Systems", **IEEE Transactions on Consumer Electronics (TCE)** , Volume: 66, Issue: 3, Aug 2020, pp. 251-260.
15. **Anirban Sengupta**, Mahendra Rathor "IP Core Steganography for Protecting DSP Kernels used in CE Systems", **IEEE Transactions on Consumer Electronics (TCE)** , Volume: 65 , Issue: 4 , Nov. 2019, pp. 506 - 515
16. **Anirban Sengupta**, E. Ranjith Kumar, N. Prajwal Chandra "Embedding Digital Signature using Encrypted-Hashing for Protection of DSP cores in CE", **IEEE Transactions on Consumer Electronics (TCE)**, Volume: 65, Issue:3, Aug 2019, pp. 398 - 407
17. **Anirban Sengupta**, Mahendra Rathor "Protecting DSP Kernels using Robust Hologram based Obfuscation", **IEEE Transactions on Consumer Electronics (TCE)**, Volume: 65, Issue: 1, Feb 2019, pp. 99-108
18. **Anirban Sengupta**, Deepak Kachave, Dipanjan Roy "Low Cost Functional Obfuscation of Reusable IP Cores used in CE Hardware through Robust Locking", **IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems (TCAD)**, Volume: 38, Issue 4, April 2019, pp. 604 - 616
19. **Anirban Sengupta**, Dipanjan Roy, Saraju P Mohanty, Peter Corcoran "Low-Cost Obfuscated JPEG CODEC IP Core for Secure CE Hardware", **IEEE Transactions on Consumer Electronics**, Volume: 64, Issue:3, August 2018, pp:365-374.
20. **Anirban Sengupta**, Dipanjan Roy, Saraju P Mohanty, "Triple-Phase Watermarking for Reusable IP Core Protection during Architecture Synthesis", **IEEE Transactions on**

Computer Aided Design of Integrated Circuits & Systems (TCAD), Volume: 37, Issue: 4, April 2018, pp. 742 - 755

21. **Anirban Sengupta**, Deepak Kachave "Spatial and Temporal Redundancy for Transient Fault Tolerant Datapath", **IEEE Transactions on Aerospace and Electronic Systems**, Volume: 54, Issue:3, June 2018, pp. 1168-1183
22. **Anirban Sengupta**, Saraju P Mohanty "Smart Electronic Systems for Consumer Electronics", **IEEE Transactions on Consumer Electronics**, Accepted, special section, 2019.
23. **Anirban Sengupta**, Saraju P Mohanty, Fernando Pescador, Peter Corcoran "Multi-Phase Obfuscation of Fault Secured DSP Designs with Enhanced Security Feature", **IEEE Transactions on Consumer Electronics**, Volume: 64, Issue:3, August 2018, pp: 356-364
24. **Anirban Sengupta**, Dipanjan Roy, Saraju Mohanty, Peter Corcoran "DSP Design Protection in CE through Algorithmic Transformation Based Structural Obfuscation", **IEEE Transactions on Consumer Electronics**, Volume 63, Issue 4, November 2017, pp: 467 - 476
25. **Anirban Sengupta**, Sandip Kundu "Securing IoT Hardware: Threat models and Reliable, Low-power Design Solutions", **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, Dec 2017, Volume: 25, Issue: 12, pp. 3265 - 3267.
26. **Anirban Sengupta**, Saumya Bhadauria, Saraju P Mohanty "TL-HLS: Methodology for Low Cost Hardware Trojan Security Aware Scheduling with Optimal Loop Unrolling Factor during High Level Synthesis", **IEEE Transactions on Computer Aided Design of Integrated Circuits & Systems (TCAD)**, Volume: 36, Issue: 4, April 2017, pp. 655 – 668.
27. **Anirban Sengupta**, Nabendu Bhui "Time-Bomb HLS Trojan for Performance Degradation Payload", **IEEE Design & Test (D&T)**, Accepted, 2025
28. **Anirban Sengupta**, Nabendu Bhui "HLS Watermarking of IP Designs using Scheduling Driven Key-based Parallel Switching Framework Integrated with Multimodal Crypto Logic", **IEEE Embedded Systems Letters (ESL)**, Accepted, 2025
29. Aditya Anshul, **Anirban Sengupta**, " HLS Trojan Detection using Machine Learning Technique", **IEEE Embedded Systems Letters (ESL)**, 2025
30. **Anirban Sengupta**, Vishal Chourasia, Nabendu Bhui "HLS Trojan Classification and its Detection Techniques for CAD based IP Designs", **IEEE IT Professional (ITPro)**, Accepted, 2025
31. **Anirban Sengupta**, Nabendu Bhui, Aditya Anshul "High Level Synthesis based Forensic Watermarking of Hardware IPs using IP Vendor's DNA Signature", **IEEE Embedded Systems Letters (ESL)**, Accepted, 2025
32. **Anirban Sengupta**, Aditya Anshul, Vishal Chourasia, Nabendu Bhui "Security Vulnerability (Backdoor Trojan) during ML Accelerator Design Phases", **IEEE IT Professional (ITPro)**, 2025, Volume 27, pp. 65-72
33. **Anirban Sengupta**, Aditya Anshul "A Survey of High Level Synthesis based Hardware (IP) Watermarking Approaches", **IEEE Design & Test (D&T)**, Volume: 41, Issue: 6, pp. 70-83, Dec 2024

34. **Anirban Sengupta**, Aditya Anshul, Vishal Chourasia, Nitish Kumar "M-HLS: Malevolent High-Level Synthesis for Watermarked Hardware IPs", **IEEE Embedded Systems Letters (ESL)**, Volume: 16, Issue: 4, pp. 497-500, Dec 2024
35. **Anirban Sengupta**, Rahul Chaurasia "Secure FFT IP using C-way Partitioning-based Obfuscation and Fingerprint", **IEEE Design & Test (D&T)**, Volume: 41, Issue: 5, pp. 55-64, October 2024
36. **Anirban Sengupta**, Aditya Anshul "Watermarking Hardware IPs using Design Parameter Driven Encrypted Dispersion Matrix with Eigen Decomposition Based Security Framework", **IEEE Access**, Volume: 12, pp. 47494-47507, 2024
37. Mahendra Rathor, **Anirban Sengupta** "Revisiting Black-Hat HLS: A Lightweight Countermeasure to HLS-aided Trojan Attack", **IEEE Embedded Systems Letters (ESL)**, Volume: 16, Issue: 2, 2024, pp. 170-173
38. Aditya Anshul, **Anirban Sengupta** "A Survey of High Level Synthesis based Hardware Security Approaches for Reusable IP Cores", **IEEE Circuits and Systems Magazine (CASM)**, Volume: 23, Issue: 4, 2023, pp. 44 - 62
39. **Anirban Sengupta**, Mahendra Rathor, Rahul Chaurasia "Biometrics for Hardware Security and Trust: Discussion and Analysis", **IEEE IT Professionals (ITPro)**, Volume: 25, Vol: 4, pp. 36 - 44, Aug 2023
40. **Anirban Sengupta**, Rahul Chaurasia "Securing IP Cores for DSP applications using Structural Obfuscation and Chromosomal DNA Impression", **IEEE Access** , Volume: 10, May 2022, pp. 50903 - 50913
41. Rahul Chaurasia, Aditya Anshul, **Anirban Sengupta** "Palmprint Biometric vs Encrypted Hash based Digital Signature for Securing DSP Cores Used in CE systems", **IEEE Consumer Electronics (CEM)** , Volume: 11, Issue: 5, September 2022, pp. 73-80
42. **Anirban Sengupta**, Mahendra Rathor "Structural Obfuscation and Crypto-Steganography based Secured JPEG Compression Hardware for Medical Imaging Systems", **IEEE Access**, Volume: 8, Issue:1, Dec 2020, pp. 6543-6565
43. **Anirban Sengupta**, Mahendra Rathor "HLS based IP Protection of Reusable Cores using Biometric Fingerprint", **IEEE Letters of the Computer Society (LOCS)** , Volume: 3, Issue: 2, July-Dec 2020, pp. 42-45.
44. **Anirban Sengupta**, Mahendra Rathor, Somesh Patil, Naukudkar Gaurav Harishchandra "Securing Hardware Accelerators using Multi-Key based Structural Obfuscation", **IEEE Letters of the Computer Society (LOCS)** , Volume: 3, Issue:1, June 2020, pp. 21-24.
45. Mahendra Rathor, **Anirban Sengupta** "Design Flow of Secured N-point DFT Application Specific Processor using Obfuscation and Steganography", **IEEE Letters of the Computer Society (LOCS)**, Volume: 3, Issue: 1, June 2020, pp. 13 - 16.
46. **Anirban Sengupta**, Mahendra Rathor "Crypto based Dual phase Hardware Steganography for Securing IP cores", **IEEE Letters of the Computer Society (LOCS)** , 2019, Volume 2 , Issue 4, pp. 32-35
47. **Anirban Sengupta**, Mahendra Rathor "Security of Functionally Obfuscated DSP core against Removal Attack using SHA-512 based Key Encryption Hardware", **IEEE Access Journal**, Volume: 7, Issue:1, 2019, pp. 4598 - 4610

48. Mahendra Rathor, **Anirban Sengupta** "Robust Logic locking for Securing Reusable DSP Cores", **IEEE Access Journal**, Volume: 7, Aug 2019, pp. 120052 - 120064
49. **Anirban Sengupta**, Deepak Kachave, "Digital Processing Core Performance Degradation Due to Hardware Stress Attacks", **IEEE Potential**, Volume: 38, Issue: 2, March-April 2019, pp. 39 - 45.
50. Deepak Kachave, **Anirban Sengupta** "Fault Tolerant DSP core datapath against Omni-directional spatial impact of SET", **IEEE Canadian Journal of Electrical and Computer Engineering**, Volume 42, issue 2, Spring 2019, pp. 102 - 107
51. Dipanjan Roy, **Anirban Sengupta** "Multi-level Watermark for Protecting DSP Kernel used in CE Systems", **IEEE Consumer Electronics**, Volume: 8 , Issue: 2 , March 2019, pp. 100 - 102
52. Dipanjan Roy, **Anirban Sengupta**, Mrinal Kanti Naskar "Signature-Free Watermark for Protecting DSP core used in CE Devices", **IEEE Consumer Electronics**, Volume 8, Issue 1, Jan 2019, pp. 92 - 94
53. **Anirban Sengupta**, Saraju P. Mohanty "Editorial: From the Editors Desk", **IEEE VLSI Circuits & Systems Letter**, Volume 5, Issue 1, Feb 2019, pp. 1.
54. **Anirban Sengupta** "Editorial: From the Editors Desk", **IEEE VLSI Circuits & Systems Letter**, Volume 5, Issue 2, May 2019, pp. 1.
55. **Anirban Sengupta**, Dipanjan Roy, Saraju Mohanty, Peter Corcoran "A Framework for Hardware Efficient Reusable IP Core for Grayscale Image CODEC", **IEEE Access Journal**, Volume: 6, Issue:1, Dec 2018, pp. 871 - 882
56. **Anirban Sengupta**, Niranjana Ray, "Audio & Video Technologies of Consumer Electronics Devices", **IEEE Consumer Electronics**, Volume: 7, Issue: 5, Sept. 2018, pp. 26 - 26.
57. Dipanjan Roy, **Anirban Sengupta**, "Obfuscated JPEG Image Decompression IP Core for Protecting Against Reverse Engineering", **IEEE Consumer Electronics**, Volume: 7, Issue: 3, May 2018, pp. 104 - 109
58. **Anirban Sengupta**, Dipanjan Roy "Framework for IP based Lossless Image Compression for Camera Systems", **IEEE Consumer Electronics**, Volume: 7, Issue: 1, pp. 119 - 124, 2018
59. Deepak Kachave, **Anirban Sengupta** "Functionally Locked IP Core in CE Hardware for Shielding against Reverse Engineering Attacks", **IEEE Consumer Electronics**, Volume: 7, Issue: 2, March 2018, pp. 111 - 114
60. Dipanjan Roy, **Anirban Sengupta**, MK Naskar "Optimizing DSP IP Cores using Design Transformation", **IEEE Consumer Electronics**, Volume: 7 , Issue: 4 , July 2018, pp. 91 - 94
61. **Anirban Sengupta**, Saraju P. Mohanty "Editorial: From the Editors Desk", **IEEE VLSI Circuits & Systems Letter**, Volume 4, Issue 1, Feb 2018, pp. 1.
62. **Anirban Sengupta**, Saraju P. Mohanty "Editorial: From the Editors Desk", **IEEE VLSI Circuits & Systems Letter**, Volume 4, Issue 2, May 2018, pp. 1.
63. S. P. Mohanty, **A. Sengupta**, P. Guturu, and E. Kougianos, "Everything You Want to Know About Watermarking: From Paper Marks to Hardware Protection", **IEEE Consumer Electronics**, Volume 7, Issue 3, July 2017, pp. 83--91.

64. **Anirban Sengupta**, Deepak Kachave "Particle Swarm Optimisation Driven Low Cost Single Event Transient Fault Secured Design during Architectural Synthesis (Invited Paper)" **IET Journal of Engineering**, Dec 2017, doi: 10.1049/joe.2016.0378.
65. **Anirban Sengupta** "Hardware Vulnerabilities and its Effect on CE Devices: Design-for-Security against Trojan", **IEEE Consumer Electronics**, Volume: 6, Issue: 3, July 2017, pp. 126 - 133.
66. **Anirban Sengupta**, Dipanjan Roy "Anti-Piracy aware IP Chipset Design for CE Devices: Robust Watermarking Approach", **IEEE Consumer Electronics**, Volume: 6, Issue: 2, April 2017, pp. 118 - 124.
67. **Anirban Sengupta**, "Hardware Security of CE Devices: Threat Models and Defence against IP Trojans and IP Piracy", **IEEE Consumer Electronics**, Jan 2017, Volume: 6, Issue: 1, pp. 130 - 133.
68. **Anirban Sengupta**, Santosh Rathlavat, Mrinal Kanti Naskar "A Firefly Algorithm Approach for Hardware Accelerators in CE Devices", **IEEE Consumer Electronics**, Volume: 6, Issue: 4, Oct. 2017
69. **Anirban Sengupta** "Mathematical Models for Latency Estimation of Loop Unrolled and Loop Pipelined CDFGs during High Level Synthesis", **IEEE VLSI Circuits & Systems Letter**, Volume 2, Issue 2, 2017, pp. 15 - 18.
70. **Anirban Sengupta**, Saumya Bhadauria, "Exploring Low Cost Optimal Watermark for Reusable IP Cores during High Level Synthesis", **IEEE Access Journal**, Invited paper, Volume:4, Issue: 99, pp. 2198 - 2215, May 2016 .
71. **Anirban Sengupta**, F. Lombardi, S.P Mohanty, M. Zwolinski, "Security and Reliability Aware System Design for Mobile Computing Systems", **IEEE Access Journal**, Volume: 4, 2016, pp. 2976 - 2980.
72. **Anirban Sengupta** "Resilient Soft IP-Core Design Against Terrestrial Transient Faults for CE Products", **IEEE Consumer Electronics**, Volume: 5, Issue: 4, Oct. 2016, pp. 129 - 131.
73. **Anirban Sengupta**, "Design Flow of a Digital IC for CE Products", **IEEE Consumer Electronics**, April 2016, Vol.5, Issue: 2, pp.58 - 62.
74. **Anirban Sengupta** "Cognizance on Intellectual Property: A High-Level Perspective", **IEEE Consumer Electronics**, Vol. 5, Issue 3, pp. 126 - 128, 2016.
75. **Anirban Sengupta** "Evolution of IP Design Process in Semiconductor/EDA Industry", **IEEE Consumer Electronics**, April 2016, Vol.5, Issue: 2, pp.123 - 126.
76. **Anirban Sengupta** "Protection of IP-Core Designs for CE Products", **IEEE Consumer Electronics**, Vol 5, pp. 83- 89, Dec 2015.

IEEE CONFERENCE PROCEEDINGS

77. Nabendu Bhui, **Anirban Sengupta** "Leveraging Multi-Layer Crypto-Logic Cross Coupled with Encoded Code Converter and Conditional Control Flow for Robust Key-Based HLS IP Watermarking", **Proceedings of 38th IEEE International System-on-Chip Conference (SOCC)**, Accepted, Dubai, 2025

78. Aditya Anshul, **Anirban Sengupta**, Vishal Chourasia "Secure Optimized Hardware IP Design Using Key-Driven Hash Slicing Based HLS Watermarking Integrated with Krill-Herd DSE", **Proceedings of 38th IEEE International System-on-Chip Conference (SOCC)**, Accepted, Dubai, 2025
79. **Anirban Sengupta**, Aditya Anshul, Nabendu Bhui "Timer-driven HLS Trojan attack on Medical System Hardware", **Proceedings of 11th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)**, Accepted, Dec 2025
80. **Anirban Sengupta**, Aditya Anshul, Nabendu Bhui "Embedding Steganography Digest using Shannon's Decomposition for Hardware Security against False IP Ownership Attack", **Proceedings of 11th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)**, Accepted, Dec 2025
81. Vishal Chourasia, **Anirban Sengupta**, Rahul Chaurasia "HLS Based Hardware Watermarking of Blur, Embossment and Sharpening Filters Using Fused Ocular Biometrics and Digital Signature", **37th IEEE International System-on-Chip Conference (SOCC)**, Dresden, Germany, Sep 2024, pp. 143-148
82. **Anirban Sengupta**, Vishal Chourasia, Aditya Anshul "HLS Scheduling Driven Encoded Watermarking for Secure Convolutional Layer IP Design in CNN", **Proceedings of 11th IEEE International Conference on Consumer Electronics (ICCE-TW)**, Taiwan, July 2024, pp. 587-588
83. **Anirban Sengupta**, Vishal Chourasia, Aditya Anshul, Nitish Kumar "Robust Watermarking of Loop Unrolled Convolution Layer IP Design for CNN using 4-variable Encoded Register Allocation", **Proceedings of 11th IEEE International Conference on Consumer Electronics (ICCE-TW)**, Taiwan, July 2024, pp. 589-590
84. Rahul Chaurasia, **Anirban Sengupta**, "HLS based Hardware Security and IP Protection", **37th International Conference on VLSI Design (VLSID)- SRF**, Kolkata, Accepted, 2024
85. **Anirban Sengupta**, Rahul Chaurasia "SWIFT: Swarm Intelligence Driven ESL Synthesis for Functional Trojan Fortification", **Proceedings of 10th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)**, Accepted, Dec 2024
86. **Anirban Sengupta**, Vishal Chourasia "HLS Based Rapid Pareto Front Search of Watermarked Convolutional Layer IP Design", **Proceedings of 10th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)**, Accepted, Dec 2024
87. **Anirban Sengupta**, Aditya Anshul "HLS Based Hardware Watermarking Using IP Seller's Superimposed Facial Anthropometric Features", **Proceedings of 10th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)**, Accepted, Dec 2024
88. **Anirban Sengupta**, Vishal Chourasia, Nitish Kumar "HLS Driven Hybrid GA-PSO for Design Space Exploration of Optimal Palmprint Biometric Based IP Watermark and Loop Unrolling Factor", **Proceedings of 10th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)**, Accepted, Dec 2024
89. **Anirban Sengupta**, Vishal Chourasia "Gen-Sign: HLS Based Watermarking Using IP Vendor's Feistel Cipher Encrypted Genomic Signature for Protecting CNN and Image Processing Filter Cores Against Piracy", **Proceedings of 10th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)**, Accepted, Dec 2024

90. **Anirban Sengupta**, Vishal Chourasia, Nilesh Kumar, Praveen Dawar "Designing Optimal Secure Hardware IPs for Consumer Electronics using Fingerprint Watermark and Evolutionary Algorithm Framework", **Proceedings of IEEE International Conference on Future Technologies for Smart Society**, Malaysia, Accepted, Aug 2024
91. Rahul Chaurasia, **Anirban Sengupta**, "Secure Accelerated Computing: High-Level Synthesis Based Hardware Accelerator Design for CNN Applications, **Proceedings of 10th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)** , Accepted, Dec 2024
92. **Anirban Sengupta**, Rahul Chaurasia, Aditya Anshul, "Hardware Security of Digital Image Filter IP Cores against Piracy using IP Seller's Fingerprint Encrypted Amino Acid Biometric Sample", **Proceedings of 8th IEEE Asian Hardware Oriented Security and Trust Symposium (AsianHOST)** , China, 2023, pp. 1-6
93. Rahul Chaurasia, Abhinav Reddy Asireddy, **Anirban Sengupta**, "Fault Secured JPEG-Codec Hardware Accelerator with Piracy Detective Control using Secure Fingerprint Template", **Proceedings of 36th IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS)** , France, Oct 2023, pp. 1-6
94. **Anirban Sengupta**, Aditya Anshul, Sumer Thakur, Chirag Kothari "Fusing IP Vendor Palmprint Biometric with Encoded Hash for Hardware IP Core Protection of Image Processing Filters", **Proceedings of 35th IEEE International Conference on Microelectronics (ICM)**, Abu Dhabi, Dec 2023, pp. 218-221
95. **Anirban Sengupta**, Aditya Anshul, Chirag Kothari, Sumer Thakur "Secured and Optimized Hardware Accelerators Using Key-Controlled Encoded Hash Slices and Firefly Algorithm Based Design Space Exploration", **Proceedings of 35th IEEE International Conference on Microelectronics (ICM)**, Abu Dhabi, Dec 2023, pp. 149-152
96. **Anirban Sengupta**, Rahul Chaurasia "Securing Fault-Detectable CNN Hardware Accelerator Against False Claim of IP Ownership Using Embedded Fingerprint as Countermeasure", **Proceedings of 9th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)** , India, Accepted, Dec 2023, pp. 147-152
97. **Anirban Sengupta**, Aditya Anshul "Key-Driven Multi-Layered Structural Obfuscation of IP Cores Using Reconfigurable Obfuscator Based Network Challenge and Switch Control Logic", **Proceedings of 9th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)** , India, Dec 2023, pp. 141-146
98. Rahul Chaurasia, **Anirban Sengupta** "Designing Optimized and Secured Reusable Convolutional Hardware Accelerator Against IP Piracy Using Retina Biometrics", **Proceedings of 9th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)** , India, Dec 2023, pp. 153-158
99. Aditya Anshul, **Anirban Sengupta** "Low-Cost Hardware Security of Laplace Edge Detection and Embossment Filter Using HLS Based Encryption and PSO", **Proceedings of 9th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)** , India, Dec 2023, pp. 135-140
100. Aditya Anshul, K Bharath, **Anirban Sengupta**, "Designing a Low Cost Secured DSP Core Using PSO-DSE Driven Steganography for CE Systems", **Proceedings of 8th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)** , India, Dec 2022, pp. 95-100

101. Aditya Anshul, **Anirban Sengupta**, "IP Core Protection of Image Processing Filters With Multi-Level Encryption and Covert Steganographic Security Constraints", **Proceedings of 8th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)** , India, Dec 2022, pp. 83-88
102. Rahul Chaurasia, **Anirban Sengupta**, "Security Vs Design Cost of Signature Driven Security Methodologies for Reusable Hardware IP Core", **Proceedings of 8th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)** , India, Dec 2022, pp. 283-288
103. Rahul Chaurasia, **Anirban Sengupta**, "Symmetrical Protection of Ownership Right's for IP Buyer and IP Vendor Using Facial Biometric Pairing", **Proceedings of 8th IEEE International Symposium on Smart Electronic Systems (IEEE – iSES)** , India, Dec 2022, pp. 272-277
104. Rahul Chaurasia, **Anirban Sengupta**, "Crypto-Genome Signature for Securing Hardware Accelerators", **Proceedings of 19th IEEE INDICON**, India, Nov 2022, pp. 1-6
105. Rahul Chaurasia, **Anirban Sengupta**, "Protecting Trojan Secured DSP cores against IP piracy using Facial Biometrics", **Proceedings of 19th IEEE INDICON**, India, Nov 2022, pp. 1-6
106. Rahul Chaurasia, **Anirban Sengupta**, "Securing Reusable Hardware IP cores using Palmprint Biometric", **Proceedings of 7th IEEE International Symposium on Smart Electronic Systems (formerly iNIS)**, India, Dec 2021, pp. 410-413
107. Mahendra Rathor, **Anirban Sengupta**, "Signature Biometric based Authentication of IP Cores for Secure Electronic Systems", **Proceedings of 7th IEEE International Symposium on Smart Electronic Systems (formerly iNIS)**, invited paper, India, Dec 2021, pp. 384-388
108. Mahendra Rathor, Vipul Mishra, **Anirban Sengupta**, "Securing IP Cores in CE Systems using Key-driven Hash-chaining based Steganography", **Proceedings of 10th IEEE International Conference on Consumer Electronics- Berlin (ICCE Berlin)**, Germany, 2020, pp. 1-4, doi: 10.1109/ICCE-Berlin50680.2020.9352192
109. Mahendra Rathor, **Anirban Sengupta**, "Obfuscating DSP Hardware Accelerators in CE Systems Using Pseudo Operations Mixing", **Proceedings of 4th IEEE International Conference on Zooming Innovation in Consumer Electronics 2020 (ZINC 2020)**, Serbia, May 2020, pp. 218-221, doi: 10.1109/ZINC50678.2020.9161775
110. **Anirban Sengupta**, Prajwal Chandra, Ranjith Kumar "Robust Digital Signature to Protect IP Core against Fraudulent Ownership and Cloning", **Proceedings of 9th IEEE International Conference on Consumer Electronics (ICCE)- Berlin**, Berlin, Sep 2019, pp. 122-124, doi: 10.1109/ICCE-Berlin47944.2019.9127238
111. **Anirban Sengupta**, Gargi Gupta, Harshit Jalan "Hardware Steganography for IP Core Protection of Fault Secured DSP Cores", **Proceedings of 9th IEEE International Conference on Consumer Electronics (ICCE)- Berlin**, Berlin, Sep 2019, pp. 97 - 102, doi: 10.1109/ICCE-Berlin47944.2019.9127237
112. **Anirban Sengupta**, Utkarsh Singh, Piyush Kalkute "Crypto based Multi-Variable Fingerprinting for Protecting DSP cores", **Proceedings of 9th IEEE International Conference on Consumer Electronics (ICCE)- Berlin**, Berlin, Sep 2019, pp. 1 - 6, doi: 10.1109/ICCE-Berlin47944.2019.9127235

113. **Anirban Sengupta**, Mahendra Rathor "Enhanced Functional Obfuscation of DSP core using Flip-Flops and Combinational logic", **Proceedings of 9th IEEE International Conference on Consumer Electronics (ICCE)- Berlin**, Berlin, Sep 2019, pp. 7 - 11, doi: 10.1109/ICCE-Berlin47944.2019.9127236
114. Dipanjan Roy, **Anirban Sengupta** "A Multi-Phase Intellectual Property Core Watermarking Approach during Architectural Synthesis", **24th Asia-South Pacific Design Automation Conference (ASP-DAC)** SRF, Japan, Accepted, Jan 2019.
115. **Anirban Sengupta**, Mahendra Rathor "Improved Delay Estimation Model for Loop Based DSP Cores", **Proceedings of 37th IEEE International Conference on Consumer Electronics (ICCE)**, Las Vegas, USA, Jan 2019, pp. 1 - 4.
116. **Anirban Sengupta**, Dipanjan Roy "Low-Overhead Highly Robust Embedded RTL Signature for DSP Core Protection: New Paradigm for Smart CE Design", **Proceedings of 37th IEEE International Conference on Consumer Electronics (ICCE)**, Las Vegas, USA, Jan 2019, pp. 1- 6.
117. **Anirban Sengupta** "Design Pruning of DSP Kernel for Multi Objective IP Core Architecture", **Proceedings of 37th IEEE International Conference on Consumer Electronics (ICCE)**, Las Vegas, USA, Jan 2019, pp. 1 - 5.
118. **Anirban Sengupta** "Message from the Conference Chair", **Proceedings of 37th IEEE International Conference on Consumer Electronics (ICCE)**, Las Vegas, USA, Jan 2019.
119. **Anirban Sengupta**, Deepak Kachave "Integrating Compiler Driven Transformation and Simulated Annealing based Floorplan for Optimized Transient Fault Tolerant DSP cores", **International Symposium on Smart Electronic Systems (formerly iNIS)**, invited paper, Hyderabad, Dec 2018, pp. 17 - 20.
120. **Anirban Sengupta**, Shubha Neema, Sri Harsha, Saraju P Mohanty, Mrinal Kanti Naskar "Obfuscation of Fault Secured DSP Design through Hybrid Transformation", **Proceedings of 17th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)**, Hong Kong, 2018, pp. 732 - 737.
121. **Anirban Sengupta**, Saraju P. Mohanty "Functional Obfuscation of DSP cores using Robust Logic Locking and Encryption", **Proceedings of 17th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)**, Hong Kong, 2018, pp. 709 - 713.
122. **Anirban Sengupta**, Hui Zhao, Saraju P. Mohanty "Energy Efficient and Hardware Secured Architectures for Smart Electronics", **Proceedings of 17th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)**, Accepted, Hong Kong, 2018.
123. **Anirban Sengupta**, Jong Lee "Message from the Technical Program Chairs", **Proceedings of 36th IEEE International Conference on Consumer Electronics (ICCE)**, Las Vegas, Jan 2018.
124. **Anirban Sengupta**, MK Naskar "High Level Synthesis Methodology for Exploring Loop Unrolling Factor and Functional Datapath ", **Proceedings of 2018 IEEE International Conference on Advanced Computation and Telecommunication**, Bhopal, Accepted, Dec 2018.

125. **Anirban Sengupta**, "Hardware Security of CE Devices: Threat Models and Defense against IP Trojans and IP Piracy", **IEEE CE Society Distinguished Lecture, IEEE CE Society Educational Activities & Webinars**, Sep 2017.
126. **Anirban Sengupta**, "Anti-Piracy aware IP Chipset Design for CE Devices", **IEEE CE Society Distinguished Lecture, IEEE CE Society Educational Activities & Webinars**, Nov 2017.
127. **Anirban Sengupta**, Sudeep Pasricha "Message from the Technical Program Chairs", **Proceedings of 3rd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)**, Dec 2017.
128. **Anirban Sengupta**, Dipanjan Roy "Multi-Phase Watermark for IP Core Protection", **Proc. 36th IEEE International Conference on Consumer Electronics (ICCE)**, Las Vegas, 2018, doi: 10.1109/ICCE.2018.8326058, pp. 1 - 3.
129. Dipanjan Roy, **Anirban Sengupta**, "Reusable Intellectual Property Core Protection for Both Buyer and Seller", **Proc. 36th IEEE International Conference on Consumer Electronics (ICCE)**, Las Vegas, 2018, doi: 10.1109/ICCE.2018.8326059, pp. 1 - 3.
130. Saumya Bhadauria, **Anirban Sengupta**, Saraju P Mohanty "Methodology for Low Cost Hardware Trojan Security Aware Scheduling With Optimal Loop Unrolling Factor During High Level Synthesis " **Cyber Security Awareness Applied Research, IIT Kanpur- New York University**, Accepted, Nov 2017.
131. **Anirban Sengupta**, "Reliability and Performance Aware SoC solutions for IoT Framework", **IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)**, June 2017.
132. **Anirban Sengupta**, "Architecture-Level Energy, Security, and Reliability Solutions for CE Digital Hardware", **36th IEEE International Conference on Consumer Electronics (ICCE)**, Las Vegas, March 2017.
133. **Anirban Sengupta**, Dipanjan Roy "Mathematical Validation of HWT Based Lossless Image Compression", **Proc. IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)**, Dec 2017, pp. 20 - 22.
134. **Anirban Sengupta**, Santosh Rathlavat, Mrinal Kanti Naskar "A Firefly Algorithm Driven Approach for High Level Synthesis", **Proc. IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)**, Dec 2017, pp. 15 - 19.
135. Deepak Kachave, **Anirban Sengupta**, Shubha Neema, Sri Harsha "Reliability and Threat analysis of NBTI Stress on DSP cores", **Proc. IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)**, Dec 2017, pp. 11 - 14.
136. Vipul Mishra, **Anirban Sengupta**, "Comprehensive Operation Chaining Based Schedule Delay Estimation during High Level Synthesis", **Proc. IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)**, Dec 2017, pp. 66 - 68.
137. **Anirban Sengupta** Madhavi Ganpatiraju, D. Das "Message from the Technical Program Chairs", **Proc. IEEE Conference on Information Technology (ICIT)**, Dec 2016, pp. xiii - xiii.

138. Deepak Kachave, **Anirban Sengupta** "Protecting Ownership of Reusable IP Core Generated during High Level Synthesis", **Proceedings of IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)**, Dec 2016, pp. 80 - 82.
139. **Anirban Sengupta**, Saumya Bhadauria, Saraju Mohanty "Embedding Low Cost Optimal Watermark During High Level Synthesis for Reusable IP Core Protection", **Proc. of 48th IEEE Int'l Symposium on Circuits & Systems (ISCAS)**, Montreal, May 2016, pp. 974 - 977.
140. **Anirban Sengupta**, Deepak Kachave "Generating Multi-Cycle and Multiple Transient Fault Resilient Design during Physically Aware High Level Synthesis", **Proc. 15th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)**, Pittsburgh, July 2016, pp. 75 - 80.
141. Saumya Bhadauria, **Anirban Sengupta**, "A High Level Synthesis Approach for Exploring Low Cost kc-cycle Transient Fault Secured Solution", **21st Asia South Pacific-Design Automation Conference (ASP-DAC)**, Accepted, Jan 2016.
142. **Anirban Sengupta**, Saumya Bhadauria "Untrusted Third Party Digital IP cores: Power-Delay Trade-off Driven Exploration of Hardware Trojan Secured Datapath during High Level Synthesis", **25th IEEE/ACM Great Lake Symposium on VLSI (GLSVLSI)**, Pennsylvania, May 2015, pp. 167 - 172 (DOUBLE BLIND REVIEW).
143. **Anirban Sengupta**, Saumya Bhadauria, "User Power-Delay Budget Driven PSO Based Design Space Exploration of Optimal k-cycle Transient Fault Secured Datapath during High Level Synthesis", **Proceedings of 16th IEEE International Symposium on Quality Electronic Design (ISQED)**, California, USA, March 2015, pp. 289 - 292 (DOUBLE BLIND REVIEW).
144. **Anirban Sengupta**, Saumya Bhadauria, "Automated Design Space Exploration of Transient Fault Detectable Datapath Based on User Specified Power and Delay Constraints", **Proceedings of 33rd VLSI - Design Automation & Test (VLSI - DAT)** Taiwan, April 2015, pp. 1 - 4 (DOUBLE BLIND REVIEW).
145. **Anirban Sengupta**, Vipul Kumar Mishra and Reza Sedaghat, "Exploration of Optimal Multi-Cycle Transient Fault Secured Datapath during High Level Synthesis based on User Area-Delay Budget", **Proceedings of 28th IEEE Canadian Conference on Electrical & Computer Engineering (CCECE)**, Halifax, May 2015, pp. 69 - 74.
146. **Anirban Sengupta**, Mrinal Kanti Naskar, "GA Driven Integrated Exploration of Loop Unrolling Factor and Datapath For Optimal Scheduling of CDFGs During High Level Synthesis", **Proceedings of 28th IEEE Canadian Conference on Electrical & Computer Engineering (CCECE)**, Halifax, May 2015, pp. 75 - 80.
147. **Anirban Sengupta** "Reliability and Security Aware RTL/System Design", **Special Session in IEEE iNIS 2015**, Participants: Intel Corporation, Broadcom Corporation (USA), Pennsylvania State University (USA) and Indian Institute of Science, **Proposal Accepted**.
148. **Anirban Sengupta**, Saumya Bhadauria, "Secure Information Processing during System level: Exploration of an Optimized Trojan Secured Datapath for CDFGs during HLS based on User Constraints", **Proceedings of IEEE iNIS 2015 Special Session**, Dec 2015, pp. 1 - 6.

149. **Anirban Sengupta**, Vipul Kumar Mishra, "Swarm Intelligence Driven Simultaneous Adaptive Exploration of Datapath and Loop Unrolling Factor during Area-Performance Tradeoff ", **Proceedings of 13th IEEE Computer Society Annual International Symposium on VLSI (ISVLSI)**, Florida, USA, July 2014, pp. 106-112 (DOUBLE BLIND REVIEW).
150. **Anirban Sengupta**, Vipul Kumar Mishra , "Integrated Particle Swarm Optimization (i-PSO): An Adaptive Design Space Exploration Framework for Power-Performance Tradeoff in Architectural Synthesis", **Proceedings of IEEE 15th International Symposium on Quality Electronic Design (ISQED 2014)**, Santa Clara, California, USA, March 2014, pp.60 - 67 (DOUBLE BLIND REVIEW).
151. **Anirban Sengupta**, Vipul Mishra, "Automated Parallel Exploration of Datapath and Unrolling Factor in High Level Synthesis using Hyper-Dimensional Particle Swarm Encoding", **Proceedings of 27th IEEE Canadian Conference on Electrical and Computer Engineering**, Toronto, May 2014, pp. 000069 - 000073.
152. **Anirban Sengupta**, Saumya Bhadauria, "Automated Exploration of Datapath in High Level Synthesis using Temperature Dependent Bacterial Foraging Optimization Algorithm", **Proceedings of 27th IEEE Canadian Conference on Electrical and Computer Engineering**, Toronto, May 2014, pp. 68- 73.
153. **Anirban Sengupta**, Vipul Mishra, " Multidimensional Encoding Based Evolutionary Exploration Approach: Adaptive Methodology for Parametric Trade-offs in High Level Synthesis for Control flow Graphs", **Proceedings of 3rd IEEE CALCON, IEEE Kolkata**, Nov 2014, pp. 43 - 46.
154. Vipul Mishra, **Anirban Sengupta**, "PSDSE: Particle Swarm Driven Design Space Exploration of Architecture and Unrolling Factors for Nested Loops in High Level Synthesis", **Proceedings of 5th IEEE International Symposium on Electronic Design (ISED)**, Dec 2014, pp. 10 - 14 (DOUBLE BLIND-REVIEW).
155. **Anirban Sengupta** and Vipul Kumar Mishra, "Time Varying vs. Fixed Acceleration Coefficient PSO Driven Exploration during High Level Synthesis: Performance and Quality ", **Proceedings of 13th IEEE International Conference on Information Technology**, Dec 2014, pp. 281 - 286 (DOUBLE BLIND REVIEW).
156. **Anirban Sengupta** and Saumya Bhadauria, "Error Masking of Transient Faults: Exploration of a Fault Tolerant Datapath Based on User Specified Power and Delay Budget", **Proceedings of 13th IEEE International Conference on Information Technology**, Dec 2014, pp. 345 - 350 (DOUBLE BLIND REVIEW).
157. **Anirban Sengupta**, Vipul Kumar Mishra, "Rapid Search of Pareto Fronts using D-logic Exploration during Multi-Objective Tradeoff of Computation Intensive Applications", **Proceedings of IEEE 5th Asian Symposium on Quality Electronic Design (ASQED)**, Malaysia, August 2013, pp. 113-122.
158. Vipul Mishra, **Anirban Sengupta** "Swarm Intelligence Driven Design Space Exploration: An Integrated Framework for Power-Performance Trade-off in Architectural Synthesis", **Proceedings of 25th IEEE International Conference on Microelectronics (ICM 2013)**, Dec 2013, pp. 1 - 4.
159. **Anirban Sengupta**, Vipul Mishra "D-logic Exploration: Rapid Search of Pareto Fronts during Architectural Synthesis of Custom Processors", **Proceedings of IEEE**

International Conference on Advances in Computing, Communications and Informatics (ICACCI-2013), August 2013, Mysore, pp. 586 - 593.

160. **Anirban Sengupta** "A Methodology for Self-Correction Scheme Based Fast Multi Criterion Exploration and Architectural Synthesis of Data Dominated Applications", **Proceedings of IEEE International Conference on Advances in Computing, Communications and Informatics (ICACCI-2013)**, August 2013, Mysore, pp.430 - 436.
161. **Anirban Sengupta** "An Architecture Synthesis Tool for Rapid Multi-Objective Exploration and RTL Circuit Generation", **ACM International Conference on Advances in Computing & Artificial Intelligence**, Accepted, 2013.
162. **Anirban Sengupta**, Reza Sedaghat, "Priority Function Driven Design Space Exploration in High Level Synthesis Based on Power Gradient Technique", **Accepted in Student Forum of 17th IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC 2012)**, Australia, pp: 25, 2012.
163. **Anirban Sengupta**, Reza Sedaghat, "Integrated Scheduling, Allocation and Binding in High Level Synthesis using Multi Structure Genetic Algorithm based Design Space Exploration System", **Proceedings of 12th IEEE/ACM International Symposium on Quality Electronic Design (ISQED 2011)**, Silicon Valley, California, USA, March 2011, pp. 486-494 (BLIND REVIEW).
164. **Anirban Sengupta**, Reza Sedaghat, "A Hybrid Fuzzy Search Approach for Fast Design Space Exploration of Multi-Objective VLSI Systems", Accepted in the Student Forum of **16th IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC 2011)**, Japan, 2011, Paper ID: SF15.
165. **Anirban Sengupta**, Reza Sedaghat "Integrated Scheduling, Allocation and Binding in High Level Synthesis for Performance-Area Tradeoff of Digital Media Applications", **Proceedings of 24th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE 2011)**, Canada, May 2011, pp. 533-537.
166. **Anirban Sengupta**, Reza Sedaghat "Priority Function based Power Efficient Rapid Design Space Exploration of Scheduling and Module Selection in High Level Synthesis", **Proceedings of 24th IEEE Canadian Conference on Electrical and Computer Engineering (CCECE 2011)**, Niagara, Canada, May 2011, pp. 538-543.
167. Reza Sedaghat, **Anirban Sengupta**, "Power Gradient Based Design Space Exploration in High Level Synthesis for DSP Kernels", **Proceedings of 23rd IEEE International Conference on Microelectronics (ICM)**, pp: 16, December 2011.
168. **Anirban Sengupta**, Reza Sedaghat "Integrated Design Space Exploration Based on Power-Performance Trade-off using Genetic Algorithm", **Proceedings of ACM International Conference on Advances in Computing and Artificial Intelligence**, 2011, pp. 76-80.
169. Reza Sedaghat, **Anirban Sengupta**, "Application Specific Processor vs. Microblaze Soft Core RISC Processor: FPGA Based Performance and CPR Analysis", **Proceedings of ACM International Conference on Advances in Computing and Artificial Intelligence**, 2011, pp.81-84.
170. Summit Sehgal, Reza Sedaghat, **Anirban Sengupta**, "Automated Design Space Exploration for DSP Applications High Level Synthesis with Stability in Competition",

Accepted for Publication, **Proceedings of 2nd IEEE Latin American Symposium on Circuits and Systems (LASCAS)**, Columbia, February 2011.

171. **Anirban Sengupta**, Reza Sedaghat, Zhipeng Zeng, "Rapid Design Space Exploration for multi parametric optimization of VLSI designs", **Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)**, Paris, France, pp: 3164-3167, June 2, 2010.
172. Zhipeng Zeng, Reza Sedaghat, **Anirban Sengupta**, "A Framework for Fast Design Space Exploration using Fuzzy search for VLSI Computing Architectures", **Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)**, Paris, France, 2010, pp: 3176-3179.
173. **Anirban Sengupta**, Reza Sedaghat, "Accelerated Exploration of Cost-Performance Tradeoffs for Multi Objective VLSI designs", **Proceedings of 22nd IEEE International Conference on Microelectronics (ICM)**, 2010, pp. 100-103.
174. **Anirban Sengupta**, Reza Sedaghat "Rapid Exploration of Power-Delay Tradeoffs using Hybrid Priority Factor and Fuzzy Search", In **Proceedings of 22nd IEEE International Conference on Microelectronics (ICM)**, Egypt, 2010, pp. 355-358.
175. **Anirban Sengupta**, Reza Sedaghat, "Fast Design Space Exploration for Multi Parametric Optimized VLSI and SoC Designs", Accepted in Student Forum of **15th IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC 2010)**, Taiwan, 2010, ID: 26.
176. **Anirban Sengupta**, Reza Sedaghat, "A Study on Architecture Optimization of the RISC Processor used for System-on Chip (SoC) design", In **Proceedings of Research Innovation Symposium, Ryerson University**, Canada, 2010, pp: 31.
177. Summit Sehgal, Reza Sedaghat, **Anirban Sengupta**, "Fault Monitoring Transformer Reliability ASIC Design based on Ringing Effect Signature Analyzer", **Proceedings of Research Innovation Symposium, Ryerson University**, Canada, 2010, pp: 32.
178. **Anirban Sengupta**, Reza Sedaghat, Zhipeng Zeng, "Hardware Efficient Design of speed optimized Power stringent Application Specific Processor", **Proceedings of 21st IEEE International Conference on Microelectronics (ICM)**, Morocco, pp: 167-170, December 22, 2009.
179. Summit Sehgal, Reza Sedaghat, **Anirban Sengupta**, Zhipeng Zeng, "Multi Parametric Optimized Architectural Synthesis of an Application Specific Processor", **Proceedings of 14th IEEE International CSI Computer Conference (CSICC)**, 2009, pp: 89-94.
180. Zhipeng Zeng, Reza Sedaghat, **Anirban Sengupta**, "A Novel Framework of Optimizing Modular Computing Architecture for multi objective VLSI designs", **Proceedings of 21st IEEE International Conference on Microelectronics (ICM)**, Morocco, 2009, pp: 322-325.